THE TDRSS DATA INTERFACE UNIT
OPERATIONS
AND
MAINTENANCE
MANUAL

Prepared for:
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1. SCOPE

This manual is intended to provide installation instruction and operational guidance for the TDRSS Data Interface Unit.

The information contained herein is provided to assist in general maintenance and troubleshooting.

1.1 INTRODUCTION

The TDRSS Data Interface (TDI)Unit was developed by the Development Engineering Group of AlliedSignal Technical Services, located in Columbia, Maryland. The unit was developed under NASA 31000 contract for the GSFC Code 531. This unit will be installed in White Sands, NM to interface between V.35 Router and Low Rate Data Switch .

1.2 GENERAL DESCRIPTION

The TDRSS Data Interface Unit has two major functions. First function is to receives F/L NRZ-L uncoded data and clock from V.35 Router and performs scrambling, differentially encoding, and convolution encoding at the rate of 1/2 with a constraint length of seven. This encoded data is then forwards to Low Rate Data Switch. Second function is to receive R/L NRZ-L uncoded, scrambled data and clock from Low Rate Data Switch and perform de-scrambling. This de-scrambled data is then forwards to V.35 Router.

The data rate and encoding selections can be selected via a front panel DIP switch.

The interface to V.35 Router is a standard V.35 and the interface to Low Rate Data Switch is RS422 balanced.

1.3 SPECIFICATION

Electrical and Physical

Input AC voltage	85-135 VAC, 47-63 Hz, single phase
Power Dissipation	20 watts max
Dimensions	17” x 1.5” x 16” (W x H x D)
Weight	7 lb.
Mounting	22” rack slide
Operating Temperature	0 degrees to 50 degrees C
Relative Humidity	20-90% without condensation

Data Interface

V.35 Router Interface (R/P J1)	V.35 is a mixture of balanced and common earth signal interface. The control lines including DTR, DSR, RTS and CTS are single wire interface, functionally compatible with RS-232 level signals. The data and clock signals including TXD, RXD, SCTE, SCT, and SCR are balanced , RS-422 like signals. The data rate up to 1.024 Mbps and 100 ohm input impedance.
TX Clock Ref (R/P J2)	TTL single ended, connector type BNC RJ178 and 50 ohm input impedance
Low Rate Data Switch Interface (R/P J3 and J4)	TTL Balanced, connector type Twinax Trompeter BJ72, symbol data rate up to 2.048 Mbps.
(R/P J5 and J6)	TTL Balanced , connector type Twinax Trompeter BJ72 and 100 ohm input impedance

2. INSTALLATION

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2.1 General

This section details procedures for installation of the TDRSS Data Interface Unit. Please read this section in its entirely before applying power to the unit

2.2 Unpacking/Visual Inspection

Remove unit from shipping carton and perform a general inspection of the unit exterior. Check for broken indicator, front panel switches, rear panel connectors, and damage to the chassis in general.

Remove the top cover and examine the unit's interior. Check for loose circuit board, power supply, and cable harness connectors, components, wiring, and connectors.

After visual inspection is completed and all items are found to be satisfactory, replace top cover.

2.3 Mounting

After performing the above unit inspection the unit can be mounted in a standard 19" rack instrumentation rack. The side rack slide is provided with the TDRSS Data Interface Unit to provide easy access to the unit's internal area.

2.4 Cooling

There are no special cooling requirements unless the ambient temperature exceeds 50 degrees C.

2.5 Cable Fabrication

Interface cables should be fabricated in accordance with related Engineering Change (EC). Recommended mating pins, and hardware for all cable assemblies are listed below.

V.35 (R/P J1)	V.35 Plug Housing
TX Clock Ref (R/P J2)	BNC Plug
Data Out (R/P J3)	Twinax Plug
Clock Out (R/P J4)	Twinax Plug
Data In (R/P J5)	Twinax Plug
Clock In (R/P J6)	Twinax Plug

2.6 Grounding

An added chassis ground lug is located on the rear panel of this unit for site installation.

3. OPERATIONS

3.1 General

The following section details the operations procedures for the unit's encoding features.

3.2 Pre-Power Up

Before applying power to the TDRSS Data Interface Unit insure the data and clock are received to the unit.

Table 3-1 contain front panel dip switch configuration definitions.

Table 3.1 Front Panel DIP Switch Definitions

DIP Switch Location	Position	Definition
SW1-1,2,3,4	OFF-OFF-OFF-OFF	1.024 Mbps
SW1-1,2,3,4	ON-OFF-OFF-OFF	512 Kbps
SW1-1,2,3,4	ON-ON-OFF-OFF	256 Kbps
SW1-1,2,3,4	ON-ON-ON-OFF	128 Kbps
SW1-1,2,3,4	ON-ON-ON-ON	64 Kbps

SW1-5	OFF	External 1.024 Mhz Clock
SW1-5	ON	Internal 1.024 Mhz Clock
SW1-6	OFF	Differentially Encoded
SW1-6	ON	Normal (Differential Encoder Out)
SW1-7	OFF	Scrambler Out
SW1-7	ON	Scrambler In
SW1-8	OFF	Convolutional Encoder Out
SW1-8	ON	Convolutional Encoder In

3.3 Control/Indicators

Item	Name	Description
1	AC Power On LED	This is a red LED which indicates the AC power on
2	AC Power Switch	This locking lever toggle switch applies 110 VAC to the TDRSS Data Interface Unit

3.4 Power Up Measurement/Adjustment

The unit's printed circuit board has a potentiometer to adjust -2Vdc output. This pot was adjusted properly prior to the shipment. Additionally, internal +5Vdc and -5Vdc power supplies outputs were adjusted properly prior to the shipment. The output voltages should be within +/- 10 %.

4. DETAILED OPERATIONS

4.1 General

This section provides a general description of the functionality of the TDRSS Data Interface Unit.

4.2 Application Hardware

The TDRSS Data Interface Unit is a single board application specific design. The Field Programmable Gate Array (FPGA) utilized in this design. A simplified block diagram which identifies the major hardware elements are shown in figure 1.

5. DRAWINGS

5.1 General

The following list of manual, assembly drawings, and logic schematics have been included in this manual to provide additional insight into the operations and maintenance of the TDRSS Data Interface Unit.

TDRSS Data Interface and TDRSS Data Interface Unit Chassis Operation and Maintenance Manual	Manual No. N/A K & H
TDI Circuit Card Assembly Drawing	1535650
TDI Circuit Card Logic Schematic	1535648

Figure 1. Simplified Block Diagram